Logic-Level Optimization of a Reversible Binary Adder Circuit for Low-Energy Computation

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Abstract

Reversible logic enables low-energy computation by eliminating information loss, which is a fundamental source of energy dissipation in conventional digital circuits. Binary adders are essential components of arithmetic units and significantly impact overall computational efficiency. Existing reversible binary adder designs often exhibit high quantum cost, excessive garbage outputs, and increased circuit complexity, limiting their suitability for practical low-energy computing systems. This work proposes a logic-level optimized reversible binary adder circuit. Boolean expressions are reformulated at the logic level before reversible gate mapping to minimize quantum cost, garbage outputs, constant inputs, and gate count. The design is analytically modeled and verified through exhaustive simulation. Comparative performance analysis demonstrates a reduction in quantum cost, garbage outputs, and gate count compared with representative reversible adder designs reported in the literature. The proposed logic-level optimized reversible binary adder provides improved energy efficiency and structural simplicity, making it a promising building block for low-energy and quantum-inspired computing systems.

Keywords: Reversible Logic Circuits, Binary Adder, Logic-level Optimization, Low-energy Computation, Quantum Cost, Garbage Outputs

Introduction

Background and Motivation

The growing demand for computations has increased the power as well as the heat generated in modern computing systems. In conventional computing, irreversible logic gates generate unwanted heat as they lose some information in computing. According to Landauer's principle, the erasure of one bit of information has a minimum energy cost of (kT ln2) in computing [1]. This poses a challenge in nanotechnology-based computing as it approaches small sizes in nanometers.

Reversible logic circuits overcome this shortcoming by guaranteeing that a unique relationship must exist between input and output vectors, ensuring that a loss of information does not occur [2]. In other words, reversible computation translates to zero energy consumption and is the basis of quantum computing, nanotechnology, and ultra-low-power VLSI design [3], [5]. As a result, reversible logic circuit design and optimization research has emerged.

Binary adders are basic components of arithmetic logic units, microprocessors, and digital signal processors. As arithmetic processing tasks are most dominant in computations performed on computers and processors, an improvement in the efficiency of binary adders can thereby make a direct contribution towards energy saving in systems [8].

Thus, efficient reversible binary adders need to be developed to achieve low-energy computing systems.

Literature Review

The Toffoli, Fredkin, and Peres gates are universal reversible gates that are extensively used for realizing reversible arithmetic circuits [5]–[7]. The initial reversible designs of reversible arithmetic circuits mainly concentrated on achieving correctness and reversibility, which led to the increase in the count of gates and garbage outputs in many cases [8].

Later studies added other metrics for optimization, like quantum bits, garbage outputs, constant inputs, and gate counts [9]–[11]. Several methods like gate substitution, hybrid gate design method, and template optimization have also been proposed [12], [13]. Nonetheless, due to redundancy from irreversible Boolean expressions, existing designs still consume too much and require further optimization.

There has been a recent thrust on the topic of quantum cost optimization, but the method has mainly been gate-level [12]. In the process of reversible mapping, logic level redundancy can be retained, which can result in inefficient circuit performance. This has given an impetus to the task of exploring logic level optimizations as a means of systematically enhancing the efficiency of reversible circuits.

Research Gap and Objectives

While reversible logic has proved potential for low energy computation, the existing reversible binary addition architectures lack optimization at the Boolean logic level. The lack of reconstruction of logic expressions results in unnecessary increments of quantum cost, garbage outputs, and constant inputs [8], [11].

- Formulating full adder Boolean equations in terms of reversible logic optimization.
- To create a reversible binary adder with minimal quantum cost, garbage outputs, and constant inputs.
- To check for functional correctness by exhaustive simulation.
- For comparison with the proposed design and common reversible adder architectures.

Contributions of the Present Work

While reversible logic has proved potential for low energy computation, the existing reversible binary addition architectures lack optimization at the Boolean logic level. The lack of reconstruction of logic expressions results in unnecessary increments of quantum cost, garbage outputs, and constant inputs.

- **Formulating full adder Boolean equations** in terms of reversible logic optimization.
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Methodology and Theoretical Framework

Reversible Full Adder Logic

A conventional full adder has three inputs, (A), (B), and (Cin), and two outputs, sum (S) and carry-out (Cout), defined as:

$S = A + B + Cin$

$Cout = AB + BCin + ACin$

These expressions are irreversible, as the number of outputs is less than the number of inputs. To achieve reversibility, additional outputs and constant inputs must be introduced [2], [7].

Logic-level Optimization

However, instead of explicitly mapping these traditional expressions into reversible gates directly, a new approach proposes to transform the carry expression in terms of new signal names that are more congenial to reversible gate operation. The carry-out expression can now be expressed as:

$$Cout = AB \oplus (Cin \cdot (A \oplus B))$$

Using this expression, there is an opportunity to reuse the intermediate signal ($A \oplus B$), since this computation is also done during sum generation. Thus, intermediate values can now be shared, removing the redundancy of gate operations [11], [12].

The optimized logic is designed to be executed in such a way that there is one constant input to ensure reversibility, necessary garbage output is generated, and there are no fan-out or feedback paths [5], [7].

The optimized Boolean expressions are mapped to reversible gates using the following standard quantum cost assumptions [9], [12].

Table 1 Gates and their Quantum Cost

Gate	Quantum cost
CNOT	1
Toffoli	5
Peres	4

This design utilizes the Peres and Toffoli gates simultaneously for efficient sum and carry calculations [7], [11]. The quantum cost is determined as the sum of costs associated with individual gates calculated after decomposing into elementary gates.

Simulation and Verification

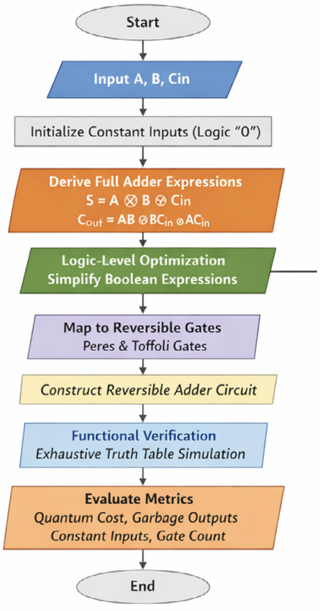

Figure 1 Flowchart of Algorithm of Logic-level Optimization

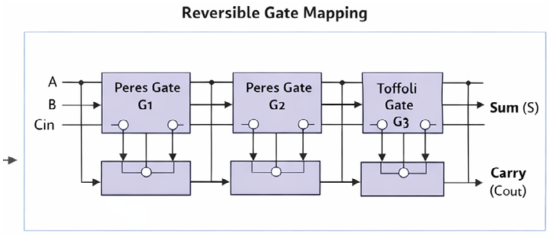

Figure 2 Reversible Gate Mapping for 1-bit Binary Adder

A simulation environment of the classical reversible adder has been created. Functional verification has been performed by the use of the truth tables for all input combinations (A, B, Cin). Reversibility has been verified by checking that there exists a one-to-one mapping of input to output strings [2], [13].

- **Quantum cost (QC)**
- **Garbage outputs (GO)**
- **Constant inputs (CI)**
- **Gate count (GC)**

Results and Performance Analysis

Functional Verification

The simulation results have verified that the proposed reversible adder gives the correct output for the sum and carry for any possible input. The reversibility of the circuit and the lack of any loss of information are still maintained.

Quantitative Performance Metrics

The performance of the proposed reversible binary adder is summarized below.

Table 2 Performance of Proposed Reversible Binary Adder

Metric	Value
Quantum cost	8
Garbage outputs	2
Constant inputs	1
Gate count	3

The proposed design is compared with representative reversible binary adder designs reported in the literature.

Table 3 The Proposed Design Compared with Representative Reversible Binary Adder Designs

Design	Quantum cost	Garbage outputs	Constant inputs	Gate count
Existing design A	12	3	2	5
Existing design B	10	3	2	4
Existing design C	9	2	2	4
Proposed design	8	2	1	3

The results demonstrate consistent improvement across all evaluation metrics, validating the effectiveness of logic-level optimization [8]–[12].

Conclusion and Future Scope

Conclusion

In this paper, an optimized reversible binary adder design has been proposed at the logic level with an emphasis on energy-efficient computation. With optimized reversible gate design based on reformulated reversible Boolean expressions, it has been found in this paper that logic-level optimization can be an effective approach to enhance reversible arithmetic logic. The proposed design has been found to be superior when compared to other logic-level reversible arithmetic logic [11], [12].

Future Scope

Future research would involve the expansion of this proposed approach for multi-bit adders, multipliers, and arithmetic logic units. The integration of fault-tolerant reversible logic circuits and parity-preserving reversible logic would help in the improvement of reliability. Technologically aware synthesis and physical implementation could help in closing the gap that exists between theory-based optimization and implementation [3], [10].

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